राष्ट्रीय प्रौद्योगिकी संस्थान रायपुर
NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR
(Institute of National Importance)
G.E. Road, Raipur – 492010 (CG)

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ADVERTISEMENT NO: ELEX/7327 **Dated: 06/12/23**

WALK- IN- INTERVIEW

Recruitment of the Project Staff through Walk-in interview (Project Associate – II, Senior Project Associate) under the following Chip to Startup (C2S), MeitY, GoI Sponsored Project of 5 years duration.

Title of the Project: Design and Development of System on Chip based next generation IoT System for Industry 4.0 with Functional Safety and Security Features.

Funding Agency Details: Chips to Startup (C2S), MeitY, GoI

Interested candidates may attend the interview with original and attested copies of all academic and experience certificates (if any) and testimonials on **Dec 18, 2023** at **11.30 AM** in the **Department of Electronics and Communication Engineering, NIT Raipur.**

Details about the position(s):

S. No.	Post	Qualification	Duration	Consolidated Salary
1	Project Associate – II No of posts: 1	ME / MTech / PhD in relevant field of Electronics / Electronics & Communication / Microelectronics / Microelectronics and VLSI Design / VLSI Design/ VLSI Design and Nanoelectronics with Experience of Design and Fabrication of Semiconductor Chip, experience to work on EDA Tools, understanding of Linux environment, Exposure to install the EDA tools, Experience to handle the VLSI training for capacity building etc.	Initial appointment is for one year, which is extendable up to duration of the project.	Rs.35,000/- + HRA (Per month) (10% increment per annum.)
2	Senior Project Associate No of posts: 1	ME / MTech / PhD in relevant field of Electronics /Electronics & Communication / Microelectronics / Microelectronics and VLSI Design / VLSI Design/ VLSI Design and Nanoelectronics with Experience of Design and Fabrication of Semiconductor Chip, experience to work on EDA Tools, understanding of Linux environment, Exposure to install the EDA tools, Experience to handle the VLSI training for capacity building etc.	Initial appointment is for one year, which is extendable up to duration of the project.	Rs.42,000/- + HRA (Per month) (10% increment per annum.)

Terms and conditions:

1. The appointment shall be on purely temporary basis and the position is coterminous with the project.

2. Initial appointment will be for 1 year which is extendable up to maximum 5 years solely based on the performance.

3. No TA/DA will be paid for attending the interview.

4. Candidates have to appear for walk-in interview/written test with bio-data, passport photos, original certificates and attested photocopies of all certificates, mark sheets, degrees and testimonials.

5. Bio-data format is being provided with this notification. The candidates are required to bring duly filled in bio-data format along with photocopies of required documents.

6. Reporting time at the Department of Electronics and Communication Engg., NIT Raipur for the Interview/written test: **Dec18, 2023** at**11.30 AM**.

7. Candidates reporting late will not be entertained.

8. The institute reserves the right to fill or not to fill any or all the posts.

Dr. Guru Prasad Subas Chandra Mishra (gpscmishra@nitrr.ac.in) & Dr. B Acharya (bacharya.etc@nitrr.ac.in)

Chief & Co-Chief Investigators, C2S

Dept. of ECE, National Institute of Technology Raipur

G.E. Road, Raipur

Chhattisgarh – 492010

India

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Paste here a recent Passport size Photograph

1. Post Applied for: Project Associate-II/ Senior Project Associate_____

2. Name of the Candidate (BLOCKLETTER):

3. Father's Name (BLOCKLETTER):

4. Mother's Name (BLOCKLETTER):

5. (a) Date of Birth: (DD/MM/YYYY)_____(b) Sex(Male/Female/Other):__

(c) Marital Status: Married/ Single (d) Category: SC/ST/OBC/PWD/Open

6. Previous Research experience: _____

7. Publication(s), if any:_____

8. GATE/ NET (if any): Qualified (Yes/No): Score:_____ Rank:_____

Specialization:_____Year:_____

9. Academic Qualification: (Starting from Standard 10 or equivalent Examination)

Name of Exam Passed	Name of the School/College/Institute/ University	Year of Passing	Discipline/ Specialization	Percentage of Marks/ CGPA

10. (a) Address for

Communication:

(BLOCKLETTER)

(b) Contact No (Mob)

(c) E-mail ID

11. Name of the Referee with email_____

_____

12. Experience on Cadence/ ___ Synopsys/ ___ Mentor/ ___ Linux /___ Others/ _____ (in years)

I do here by declare that the information furnished in this application is true to the best of my knowledge and belief. If selected, I promise to abide by the rules and regulations of the Institute.

Date:

Note- If any information is required, extra A4 sheet may be attach.

Place: **Full Signature of the Applicant**

ELIGIBILITY

1. M.Tech./M.E./ equivalent in Microelectronics & VLSI / or E & TC with strong exposure to VLSI Design, CAD Tools with at least 6.5 CGPA or 60 percent marks in aggregate from a recognized technical institute or university/ university as a Full time program.

2. B. Tech/B.E./ in E & TC with at least 6.5 CGPA or 60 percent marks in aggregate from a recognized technical institute or university/as a Full time program.

APPLICATION CHECKLIST (AT THE TIME OF INTERVIEW)

The completed application (duly signed) must be produced with following self-attested documents at the time of interview.

i) Photocopy of marks sheet/Grade card of the secondary (10), higher secondary (10+2),

ii) Photocopy of the certificate/provisional certificate of B.E/B.Tech, M.E/M. Tech, Ph.D examination.

iii) Photo copy of proof of date of birth.

iv) No-objection certificate from the present employer, if applicable.